REMARKS

Claims 5-13, 36-41and 43-64 are now pending in this application. All the claims stand rejected under 35 USC §102 or §103.

A detailed response to these rejections follows. However, applicant reserves all applicable rights not exercised in connection with this response, including, for example, the right to swear behind one or more of the cited references, the right to rebut any tacit or explicit characterization of the references, and the right to rebut any asserted motivation for combination. Applicant makes no admission regarding the prior art status of the cited references, regarding them only as being of record in the application.

Information Disclosure Statement

Applicant submits respectfully a Supplemental Information Disclosure Statement and accompanying 1449 Form were filed on June 30, 2003. However, applicant has not received evidence of its consideration. Accordingly, applicant requests that the submitted references be considered and that an initialed copy of the 1449 Form be returned with the next official communication.

Response to §102 Rejections

The Examiner rejected claims 5, 6, 43, 47, 54, 57, and 60-64 under 35 USC §102(e) as anticipated by Mikagi (U.S. Patent 6,153,507), specifically citing Figure 6a, element 107a; and Fig. 6c, element 108a (as see in Figs 7A-TF).

In response to the rejection of claims 5 and 6, applicant submits respectfully that Mikagi fails, at a minimum, to teach "forming a diffusion-barrier lining around the conductive structure after forming the conductive structure, with at least a portion of the diffusion-barrier lining contacting the surface of the conductive structure [that confronts the substrate.]" as claims 5 and 6 require. Exemplary support for this aspect of the claims is found at Figures 5 and 6 of the application.

In contrast to this requirement, Mikagi's alleged barrier element 108a, as shown in both Figs 6A-6D and 7A-7D does not contact the substrate-confronting surface of its conductor 107a.

Indeed, in both these figures, Mikagi shows the substrate-confronting surface of conductor 107a (its bottom surface) in contact with alleged barrier element 106a. However, barrier element 106a is formed before formation of conductor 107a, not afterward as specified in claims 5 and 6.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §102 rejection of claims 5 and 6.

Claims 43, 47, 50, 52, 54, and 57 also distinguish from Mikagi. For example, each of these claims specify formation of at least a portion of a diffusion-barrier lining or a layer of tungsten silicon nitrogen on at least one exposed portion of a prior-formed conductive structure that confronts the integrated circuit substrate.

Specifically (and with emphasis added), claim 43 recites "forming a diffusion-barrier lining on exposed portions of the first conductive structure **after** forming the first conductive structure, with at least one of the exposed portions having a surface confronting the integrated circuit substrate." Claim 47 recites "forming a diffusion-barrier lining on exposed portions of the conductive structure **after** forming the conductive structure, with at least one of the exposed portions having a surface confronting the integrated circuit substrate." Claim 50 recites "forming a diffusion-barrier lining on substantially all exposed portions of the conductive structure **after** forming the conductive structure by forming a layer of tungsten silicon nitrogen over substantially all of the exposed portions of the conductive structure, with at least one of the exposed portions having a surface confronting the integrated circuit substrate." Claim 52 recites "forming a diffusion-barrier lining on ... the conductive structure **after** forming the conductive structure by forming a layer of tungsten silicide over substantially all of the exposed portions of the conductive structure, with at least one of the exposed portions having a surface confronting the integrated circuit substrate. Claim 54 recites "forming a diffusion-barrier lining on substantially all exposed portions of the conductive structure **after** forming the conductive structure... at least one of the exposed portions [having] a surface confronting the integrated circuit substrate. And, claim 57 recites "forming a diffusion-barrier lining on exposed portions of the conductive structure **after** forming the conductive structure, with at least one of the

exposed portions having a surface confronting the integrated circuit substrate. Again, exemplary support for this aspect of the invention is found in Figures 5 and 6.

In contrast, Mikagi appears only show that prior to formation of its barrier element 108a, its conductor 107a has only lateral exposed surfaces in Figure 6A-6D and top exposed surfaces in Figures 7A-7D. Thus, none of Mikagi's exposed conductor surfaces confront its substrate. Therefore, its barrier element 108a is not formed on any exposed conductor surfaces that confronts the substrate.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §102 rejection of claims 43, 47, 50, 52, 54, and 57.

Claims 60-64 also distinguish from Mikagi. For example, each of these claims recites "forming a conductive structure over a substrate, with the conductive structure having a first surface spaced from and in a confronting relationship with the substrate" and "forming a diffusion barrier **after** forming the conductive structure, with at least a first portion of the diffusion barrier between the surface of the conductive structure and the substrate. (Emphasis added.)

In contrast, Mikagi's conductor 107a is shown in Figures 6A-6D and 7A-7D as having only one surface confronting its substrate—its lower surface. The only barrier element formed after the formation of conductor 107a is barrier element 108a and that element is not between the lower surface of conductor 107a and the substrate. Thus, Mikagi fails, at a minimum, to meet this aspect of claims 60-64.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §102 rejection of claims 60-64.

Response to §103 Rejections

Additionally, the Examiner rejected the remaining dependent claims of the application under 35 USC §103(a) as obvious over Mikagi in view of one or more other references. Specifically, claim 8 was rejected over Mikagi as applied to claims 5, 6, 43, 47, 54, and 57 in view of Jin (Materials Research Society: 1997); claims 9, 12, and 13 were similarly rejected over Mikagi in view of Beinglass (U.S. Patent 5,940,733); claims 10, 11, 48-53, 55, 56, 58, and 59

were rejected over Mikagi and Beinglass as applied to claims 5, 6, 9, 12, 13, 43, 47, 54, and 57 in view of Hirata (NTT System Electronics Laboratories); claims 44 and 45 were rejected over Mikagi in view of Zhao (U.S. Patent No. 5,674,787); and claim 46 was rejected over Mikagi and Zhao in view of Abraham (U.S. Patent 6,004,884).

In response, applicant submits respectfully that these rejection are all based on Mikagi, which as demonstrated above, fails to teach at least one feature of each of the independent claims on which the current claims depend.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §103 rejections based on Mikagi.

Conclusion

In view of the remarks and further highlighted shortcomings of the principle reference Mikagi, applicant requests respectfully that the Examiner reconsider the application. Additionally, applicant requests respectfully that the Examiner initiate a telephonic interview with its patent counsel, Eduardo Drake, to discuss resolution of any issues that may delay allowance of the application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
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Amy Moriarty
Name

_____
Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kie Y. Ahn et al.	Examiner: William D. Coleman
Serial No.:	09/484,303	Group Art Unit: 2823
Filed:	January 18, 2000	Docket: 303.648US1
Title:	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/032197 6211073	February 27, 1998	303.459US1	METHODS FOR MAKING COPPER AND OTHER METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/817447	March 26, 2001	303.459US2	METHODS FOR MAKING COPPER AND OTHER METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/128859 6284656	August 4, 1998	303.473US1	COPPER METALLURGY IN INTEGRATED CIRCUITS
09/946055 6614099	September 4, 2001	303.473US2	COPPER METALLURGY IN INTEGRATED CIRCUITS
09/145012 6288442	September 1, 1998	303.505US1	INTEGRATED-CIRCUIT WITH OXIDATION-RESISTANT POLYMERIC LAYER
09/256123 6211049	February 24, 1999	303.505US2	FORMING SUBMICRON INTEGRATED-CIRCUIT WIRING FROM GOLD, SILVER, COPPER AND OTHER METALS

09/256124 6208016	February 24, 1999	303.505US3	FORMING SUBMICRON INTEGRATED-CIRCUIT WIRING FROM GOLD, SILVER, COPPER AND OTHER METALS
09/789091	February 20, 2001	303.505US4	INTEGRATED-CIRCUIT WITH OXIDATION-RESISTANT POLYMERIC LAYER
09/854540	May 14, 2001	1303.013US1	COPPER DUAL DAMASCENE INTERCONNECT TECHNOLOGY
09/488098 6429120	January 18, 2000	303.618US1	METHOD AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS
09/483869 6420262	January 18, 2000	303.664US1	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
09/483881	January 18, 2000	303.672US1	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION
09/484002 6376370	January 18, 2000	303.673US1	PROCESS FOR PROVIDING SEED LAYERS FOR USING ALUMINUM, COPPER, GOLD AND SILVER METALLURGY
09/584157 6674167	May 31, 2000	303.685US1	MULTILEVEL COPPER INTERCONNECT WITH DOUBLE PASSIVATION
10/117041	April 5, 2002	303.673US2	INTEGRATED CIRCUIT AND SEED LAYERS
10/196078 6743716	July 16, 2002	303.664US2	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
10/196081	July 16, 2002	303.664US3	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION

10/211855 6756298	August 1, 2002	303.618US2	METHOD AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS
10/842042	May 7, 2004	303.618US3	METHOD AND APPARATUS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS
10/195965	July 16, 2002	303.664US4	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
10/721920	November 24, 2003	303.685US2	MULTILEVEL COPPER INTERCONNECT WITH DOUBLE PASSIVATION
10/789882	February 27, 2004	303.673US3	INTEGRATED CIRCUIT AND SEED LAYERS
10/854552	May 26, 2004	303.664US5	STRUCTURES AND METHODS TO ENHANCE COPPER METALLIZATION
10/842243	May 10, 2004	1303.013US2	COPPER DUAL DAMASCENE INTERCONNECT TECHNOLOGY
	August 30, 2004	303.672US2	SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION
	August 31, 2004	303.648US2	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

Respectfully submitted,

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By Applicants' Representatives,

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Date 10 Sept. 2004 By

Eduardo E. Drake
Reg. No. 40,594

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Name Amy Moriarty

Signature